ATTACHMENT A

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In Application Serial No. 10/677,006
Filed September 30,2003

DECLARATION OF DAVID R. EVANS UNDER 37 CFR §1.132

I, David Russell Evans, Ph.D., hereby declare as follows:

1. My residence address is 7574 S.W. 179th Street, Beaverton, Oregon 97007.

2. Since April 1, 1999 I have been employed by Sharp Laboratories of America, Inc. ("SLA"), 5700 N.W. Pacific Rim Boulevard, Camas, Washington 98607, and between 1993 and April 1, 1999 I was employed by SLA's predecessor company, Sharp Microelectronics Technology, Inc. ("SMT"), located at the same address. My titles at SMT (until April 1, 1999) were, originally, Principal Engineer and, later, Senior Member of the Technical Staff, and my title at SLA, since April 1, 1999, is Senior Manager. My responsibilities include developing advanced process technologies to improve microelectronics fabrication.

3. I have read the claims for the patent application in question, Wei Gao et al., Serial Number 10/677,006 (the Applicant). I have read the relevant parts of the Office Action dated December 10, 2004, where claims 1 through 3 have been rejected as anticipated by US Patent 6,489,645 (Uchiyama). I have also read the relevant parts of the Office Action, with respect to claims to the following rejections:

the rejection of claim 4-5 as obvious with respect to Uchiyama in view of Ma ("High-k Dielectrics for Scaled CMOS Technology);

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the rejection of claim 6-7 as unpatentable over Uchiyama in view of Gonzalez (US 6,468,852);

the rejection of claims 8-9 as unpatentable over Uchiyama in view of Gonzalez and Wilson et al. (Handbook of Multilevel Metallization for Integrated Circuits;

the rejection of claim 10 and 11 as unpatentable over Uchiyama, in view of Ma.

4. In claims 1 and 10, and as shown in Figs 7 and 10, the Applicant recites a FET with a dielectric layer (112 in Fig. 7, or 416 in Fig. 10). A gate electrode made from niobium monoxide (124 in Fig. 7, or 418 in Fig. 10) overlies the dielectric layer. The specification, on page 4, discusses the different phases of niobium oxide. Since Nb2O5 and NbO2 are insulators, and niobium monoxide (NbO) is a conductor, only NbO can be used as a gate electrode.

5. Uchiyama's invention concerns a memory device that avoids the point charge defects associated with some ferroelectric superlattice films, or the high-temperature processing associated with layered superlattice films. Diffusion is another problem associated with superlattice materials, which has conventionally been solved with the use of relatively thick buffer layers. These thick buffer layers act to decrease memory density. Uchiyama's solution involves the use of a thin interface buffer layer interposed between the electrode and the superlattice layer. In one embodiment, Uchiyama mentions that niobium oxide can be used as either the superlattice material or the buffer layer (see column 11, line 33 through column 12, line 20).

6. Uchiyama does not specifically describe the phase of niobium oxide that he uses. However, if niobium oxide is to be used as a

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buffer between an electrode and a superlattice material it must necessarily be insulating in nature. It is well-known that niobium forms three stoichometric oxides, namely, NbO, NbO2, and Nb2O5. Of these, niobium dioxide and niobium pentoxide are insulating and, accordingly, are suitable for use as buffer layers as taught by Uchiyama. In contrast, niobium monoxide is conductive and, therefore, cannot form an insulating buffer layer, by definition. Indeed, if niobium monoxide were used in this application, the resulting device would not be as described by Uchiyama, but would rather be a simple ferroelectric capacitor having a niobium oxide top or bottom electrode or both. Therefore, Uchiyama's invention cannot be practiced if his niobium oxide is in any way interpreted to be niobium monoxide.

7. Likewise, as a conductor, NbO has no demonstrable ferroelectric properties, and therefore it cannot be used as a component layer in a ferroelectric superlattice.

8. Section 3 of the Office Action states that Uchiyama describes a gate structure with a niobium monoxide gate. This assertion appears to be incorrect for a number of reasons. First, Uchiyama never mentions the material niobium monoxide (NbO). As mentioned above, Uchiyama only mentions the term "niobium oxide", and my opinion is that phase used by Uchiyama cannot be conductive.

In a single sentence at column 14, line 51-54, Uchiyama mentions that his invention is applicable to a ferroelectric FET. I interpret this statement to mean that the invention is applicable to one-transistor memory devices. However, within this context, the device taught by Uchiyama is not essential to the intrinsic operation of the transistor itself, but merely constitutes a separate device with some components physically merged with the transistor structure for the purpose of integration. In

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contrast, for the Applicant's invention the nature of the niobium oxide electrode is fundamental to the characteristics and operation of the transistor device. Accordingly, Uchiyama mentions a few conventional electrode metals (column 6, line 56-66), but he never mentions niobium oxide (of any phase) as a possible gate material.

9. In summary, it is my opinion that Uchiyama does not describe niobium monoxide, or the use of niobium monoxide as a gate material. Therefore, I do not see how Uchiyama can anticipate the Applicant's invention.

10. With respect to the obviousness rejections, regardless of whether the other references describe a high-k dielectric, a capping layer, or a TiN capping layer material, none of the various combinations cited in the Office Action appear to make the inventions of either claim 1 or claim 10 obvious. As I stated above, Uchiyama does not describe a niobium monoxide gate material. None of the other references mention niobium monoxide as a gate material, or suggest that Uchiyama's invention can be modified to use a conductive phase of niobium oxide as a gate electrode material. Therefore, I do not believe that any of the combination of references cited in the Office Action makes the Applicant's NbO gate obvious.

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11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

2/Mar/2005

Date

David R. Evans

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